signal, the error signal being applied to the tuning input.

2. (Unchanged) The phase lock loop of claim 1 wherein the second signal comprises a frequency different from the frequency of the oscillator output.

3. (Unchanged) The phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal.

4. (Unchanged) The phase lock loop of claim 1 further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the frequency of the oscillator output and a harmonic of the second signal.

5. (Unchanged) The phase lock loop of claim 3 further comprising a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector.

6. (Unchanged) The phase lock loop of claim 1 further comprising a charge pump disposed between the phase detector and the oscillator.

7. (Unchanged) The phase lock loop of claim 1 further comprising a loop filter disposed between the phase detector and the oscillator.

8. (Unchanged) The phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, and the second signal comprises a frequency different from the frequency of the oscillator output, the phase lock loop further comprising a bandpass

filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the frequency of the oscillator output and a harmonic of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector, a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

9. (Unchcanged) A phase lock loop, comprising:
a tunable oscillator having a tuning input;
a subsampling mixer having coupled the oscillator; and
a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

10. (Unchanged) The phase lock loop of claim 9 wherein the oscillator comprises a voltage controlled oscillator.

11. (Unchanged) The phase lock loop of claim 9 further comprising a bandpass filter coupled between the subsampling mixer and the first input of the phase detector.

12. (Unchanged) The phase lock loop of claim 9 further comprising a limiter coupled between the bandpass filter and the first input of the phase detector.

13. (Unchanged) The phase lock loop of claim 9 further comprising a charge pump coupled between the phase detector output and the tuning input of the oscillator.

14. (Unchanged) The phase lock loop of claim 9 further comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator.

15. (Unchanged) The phase lock loop of claim 9 wherein the oscillator comprises a voltage controlled oscillator, the phase lock loop further comprising a bandpass filter coupled to the subsampling mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

16. (Unchanged) A phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal;

filter means for filtering the mixed signal to generate a difference signal between the frequency of the first signal and a harmonic of the second signal; and

detector means for detecting a phase difference between the filtered mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

17. (Unchanged) The phase lock loop of claim 16 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

18. (Unchanged) The phase lock loop of claim 16 wherein the second signal comprises a frequency different from the frequency of the oscillator means.

19. (Unchanged) The phase lock loop of claim 16 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

20. (Unchanged) The phase lock loop of claim 16 further comprising means for sourcing current to the tuning means responsive to the error signal.

21. (Unchanged) The phase lock loop of claim 16 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

22. (Unchanged) The phase lock loop of claim 16 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, and the second signal comprises a frequency different from the frequency of the oscillator means, the phase lock loop further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

30. (Unchanged) A method of upconverting an input signal, comprising:

generating a first signal having a tunable frequency;

mixing the first signal with a second signal to produce a mixed signal;

filtering the mixed signal to generate a difference signal between the frequency of the first signal and a harmonic of the second signal;

generating an error signal as a function of a phase difference between the mixed signal and the input signal; and

tuning the first frequency with the error signal.

31. (Unchanged) The method of claim 30 further comprising modulating a carrier with a third signal, the modulated carrier comprising the input signal.

32. Unchanged) The method of claim 30 further comprising transmitting the tuned first signal into free space.

33. (Unchanged) The method of claim 32 wherein the second signal comprises a frequency different from the frequency of the first signal, the method further comprising limiting the filtered mixed signal before generating the error signal, and filtering the error signal before using it to tune the first frequency.

34. (Unchanged) The method of claim 30 wherein the second signal comprises a frequency different from the frequency of the first signal.

35. (Unchanged) The method of claim 30 further comprising limiting the filtered mixed signal before generating the error signal.

36. (Unchanged) The method of claim 30 further comprising filtering the error signal before using it to tune the first frequency.